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09/780,477	02/12/2001	Akira Yamazaki	57454-011	6387

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/780,477	Applicant(s) YAMAZAKI ET AL.	
	Examiner Quan Tra	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the amendment filed 06/25/2003. The rejection unde 35 U.S.C. 112, first paragraph, in previous office action is maintained.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-24 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification fails to teach the second power on detection circuit performing detection of the power on independently of the voltage level of the first power supply voltage, and the specification fails to teach the first power on detection circuit performing detection of the power on independently of the voltage level of the second power supply voltage.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 1-24 are indefinite because the specification fails to show the second power on detection circuit performing detection of the power on independently of the voltage level of the

first power supply voltage, and the specification fails to shows the first power on detection circuit performing detection of the power on independently of the voltage level of the second power supply voltage. Therefore, the limitation "independently" of the voltage level of the first or second power supply voltage is not given any patentable weight.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 7, 19, 21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Crotty (USP 6160431).

Because the specification fails to teach "the second power on detection circuit performing detection of the power on independently of the voltage level of the first power supply voltage", and "the first power on detection circuit performing detection of the power on independently of the voltage level of the second power supply voltage", the limitation "independently" of the voltage level of the first or second power supply voltage is not given any patentable weight.

As to claim 1, Crotty discloses in figure 6 a semiconductor integrated circuit device comprising: a first power-on detection circuit (210, 220) responsive to a first power supply voltage (Vcc1) for detecting power-on of the first power supply voltage to activate a first power-on detection signal (VD1) according to a result of detection; a second power-on detection circuit (630, 640) responsive to a second power supply voltage (Vcc2) for detecting power-on of

the second power supply voltage to activate a second power-on detection signal (VD2) according to a result of detection; and a main power-on detection circuit (650) coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active (low level) from activation (low level) of a first activated power-on detection signal (the signal is active when at low level) of the first and second power-on detection signals until inactivation (high level) of a second activated power-on detection signal of the first and second power-on detection signals (column 9 teaches circuit 650 can be an AND gate).

As to claim 2, it is inherent that the main power-on detection circuit (OR gate 950) comprises a first reset element (one of the elements, e.g. transistors, which is not shown, in the OR gate which receiving one of the input signal) responsive to activation of the first power-on detection signal for resetting a first node (output of the OR gate) to a first voltage level, a second reset element (the other element in the OR gate which receiving the other input signal) responsive to activation of the second power on detection signal for resetting the first node to the first voltage level, and a circuit (the first inverter in the delay circuit 940, see figure 5a) coupled to the first node and receiving the first power supply voltage (Vcc1 . Column 2 teaches that Vcc1 is used for input/output logic circuits. Therefore, the delay circuit must be coupled to Vcc1) as an operation power supply voltage for inactivating the main power-on detection signal and setting the first node to a second voltage level when both of the first and second power-on detection signals are inactivated.

As to claim 3, figure 9 shows a converting voltage application detection circuit (940) receiving a voltage (Vcc1) different in voltage level from the second power supply voltage

(Vcc2) as an operation power supply voltage for converting a voltage level of the main power-on detection signal to generate a converted voltage application detection signal.

As to claim 7, Crotty's column 2, line 14-25 teaches that the first and second power supply voltages are applied to a storage device (microprocessors which inherent comprising memory circuits), and the second power supply voltage (Vcc2) is applied to a logic circuit (internal logic circuits).

Claim 19 recites similar limitations of one of the claims above. Therefore, they are rejected for the same reasons.

As to claims 21 and 23, it is clearly see that the activation (low) of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation (high) of the detection signal indicates stability of the corresponding power supply voltage.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 11, 16-18, 20, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crotty (USP 6160431).

As to claims 11, 16 and 17, figure 9 shows an internal voltage application detection circuit (210) for activating an internal voltage power-up detection signal according to a voltage level of an internal voltage (Vcc1); a power-on detection circuit (630) for detecting power-on of a second power supply voltage (Vcc2) to activate a power-on detection signal according to a

result of detection; and a main power-on detection circuit (950) responsive to the internal voltage power-up detection signal and the power-on detection signal for generating a main power-on detection signal rendered active while at least one of the internal voltage power-up detection signal and the power-on detection signal is active. Thus, figure 9 shows all limitations of the claim except for an internal voltage generation circuit receiving a first power supply voltage and generating the internal voltage. However, it is notorious well known in the art that a voltage step down circuit is for generating a voltage that is lower than its input voltage or a boost voltage circuit is for generating a voltage which is higher than the input voltage of the boost circuit. It is also well known in the art that 5 Volts is a common voltage level that used to supply integrated circuit. Crotty teaches Vcc1 is 3.3 volts. Therefore, One skill in the art would have motivated to use a voltage step down circuit to convert the 5 volts supply voltage to 3.3 volts for the purpose of generating the desired Vcc1.

As to claim 18, column 2 teaches the first and second power supply voltages are applied to a storage device (microprocessor) and the second power supply voltage is applied to a logic circuit (internal logic circuits), the storage device and said logic circuit being integrated on a common semiconductor chip.

Claim 20 recites similar limitation of claim 11. Therefore, it is rejected for the same reasons.

As to claims 22 and 24, it is clearly see that the activation (low) of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation (high) of the detection signal indicates stability of the corresponding power supply voltage.

Allowable Subject Matter

10. Claims 4-6, 8-10, 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4-6, 8-10, 12-15 would be allowable because the prior art fails to teach or suggest a circuit such as figure 7 comprising: an internal voltage generation circuit for generating an internal voltage (Vpp) from the first power supply voltage, the internal voltage differing in voltage level from the second power supply voltage; and an internal circuit reset when said main power-on detection signal (/POROH) is activated, and activated, when the main power-on detection signal is inactivated, for converting a signal (SigL) having an amplitude of the second power supply voltage level into a signal having an ,amplitude of the internal voltage level. voltage is a down-converted voltage lower in voltage level than said first power supply voltage.

Response to Arguments

11. Applicants' arguments have been fully considered but they are not persuasive. Applicants argue that "The specification states that each of the power-on detection circuits detect power-on of the respective DRAM power supply voltage. There is no influence of power supply voltage VDDH on power-on detection circuit 10, and no influence of power supply voltage VDDL on power on detection circuit 11". However, it is not seen where the specification that teaches "there is no influence of power supply voltage VDDH on power-on detection circuit 10, and no influence of power supply voltage VDDL on power on detection circuit 11". It has been known in the art that a power supply voltage can be generated by another power supply voltage by using a voltage step down circuit or a voltage boosting circuit. Therefore, one skill in the art will not

sure that VDDL and VDDH are independent from each other unless the specification clearly teach so. Thus, claims 1-24 are non-enable because the specification fails to teach VDDH and VDDL are independent from each other.

Applicants further argue that the "active state of a Power-On Reset signal (POR1, POR2) must be a high state". The Examiner respectfully disagrees. One can define a level of a signal either as an "active state" or inactive state depending on his or her preference. Applicants define a low level of a signal as an "active state". Therefore, a low level of the Power-On Reset signal (POR1, POR2) is interpreted as an active state of that signal as defined by the Applicants.

Applicants further request for evidence that teaches method for using voltage stepdown circuit for generating a desired voltage which is lower than the supply voltage". US Patent 5457421 is one of the example of using a voltage stepdown circuit for generating internal voltage which is lower than the supply voltage.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
July 31, 2003

Terry D. Cunningham
Primary Examiner